

Mems Oscillator, High Performance Differential Oscillator, LVPECL and LVDS, Standard Frequencies

IM842 Series

Features:

- Standard Frequencies from 25.000 MHz to 212.500 MHz
- Direct pin to pin drop-in replacement for industry-standard packages
- 0.6 pSec RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- LVPECL and LVDS output signaling types
- Industry-standard package 3.2 x 2.5, and 5.0 x 3.2 mm x mm
- Pb-free, RoHS and REACH compliant

Typical Applications:

- Fibre Channel
- Server and Storage
- GPON, EPON
- 100M / 1G /10G Ethernet

Electronic Specifications:

Frequency Range	Standard Frequencies 25.000 MHz to 212.500 MHz	See List of Supported Frequencies (sheet 2)
Frequency Stability	See Part Number Guide	Inclusive of all changes in Operating Temp. Range, Load, and Voltage.
First Year Aging	±2.0 ppm max	+25°C ±2.0°C
10 Years Aging	±5.0 ppm max	+25°C ±2.0°C
Operating Temperature	See Part Number Guide	
Supply Voltage (Vdd) ±10%	See Part Number Guide	
Input Voltage High	70% of Vdd min	Pin 1, OE or \overline{ST}
Input Voltage Low	30% of Vdd max	Pin 1, OE or \overline{ST}
Input Pull-up Impedance	100 kΩ typ., 250 kΩ max 2.0 MΩ min	Pin 1, OE logic high or logic low, or \overline{ST} logic high Pin 1, \overline{ST} logic low
Start-up Time	6.0 mSec typ., 10.0 mSec max	Measured from the time Vdd reaches its rated minimum values
Resume Time	6.0 mSec typ., 10.0 mSec max	Measured from the time \overline{ST} pin crosses 50% threshold.
Symmetry	45%/55%	

LVPECL, DC and AC Characteristics

Current Consumption	61 mA typ., 69 mA max	Excluding Load Termination Current, Vdd = +3.3 V or +2.5 V
OE Disable Supply Current	35 mA max	OE = Low
Output Disable Leakage Current	1 μA max	OE = Low
Standby Current	100 μA max	\overline{ST} = Low, for all Vdds
Maximum Output Current	30 mA max	Max average current drawn from OUT+ or OUT-
Logic "1"	Vdd -1.1 min / Vdd - 0.7 max	See figure 1(a)
Logic "0"	Vdd -1.9 min / Vdd - 1.5 max	See figure 1(a)
Output Differential Volt.Swing	1.2 V min. 1.6V typ., 2.0 V max	See figure 1(b)
Rise/Fall Time	300 pSec typ, 500 pSec max	20% to 80%, see figure 1(a)
OE Enable/Disable Time	115 nSec max	F = 212.50 MHz – For other frequencies, T _{oe} = 100nSec + 3 period
RMS Period Jitter	1.2 pSec typ., 1.7 pSec max 1.2 pSec typ., 1.7 pSec max 1.2 pSec typ., 1.7 pSec max	F = 100.00 MHz, Vdd = +3.3 V or +2.5 V F = 156.25 MHz, Vdd = +3.3 V or +2.5 V F = 212.25 MHz, Vdd = +3.3 V or +2.5 V
RMS Phase Jitter (random)	0.60 pSec typ, 0.85 pSec max.	F = 156.25 MHz, Integration Bandwidth = 12 kHz to 20 MHz all Vdds

LVDS, DC and AC Characteristics

Current Consumption	47 mA typ., 55 mA max	Excluding Load Termination Current, Vdd = +3.3 V or +2.5 V
OE Disable Supply Current	35 mA max	OE = Low
Differential Output Voltage	250mV min, 350mV typ. 450mV max	See Figure 2
Output Disable Leakage Current	1 μA max	OE = Low
Standby Current	100 μA max	\overline{ST} = Low, for all Vdds
VOD Magnitude Change	50 mV max	See Figure 2
Offset Voltage	1.125 mV, 1.200 mV typ. 1.375 mV max	See Figure 2
VOS Magnitude Change	50 mV max	See Figure 2
Rise/Fall Time	495 pSec typ. 600 pSec max	20% to 80%, See Figure 2
OE Enable Time/Disable Time	115 nSec max	F = 212.25 MHz, For other Frequencies, T _{oe} =100nSec + 3 period
RMS Period Jitter	1.2 pSec typ, 1.7 pSec max 1.2 pSec typ, 1.7 pSec max 1.2 pSec typ, 1.7 pSec max	F = 100.00 MHz, Vdd = +3.3 V or +2.5 V F = 156.25 MHz, Vdd = +3.3 V or +2.5 V F = 212.25 MHz, Vdd = +3.3 V or +2.5 V
RMS Phase Jitter (random)	0.60pSec typ., 0.85 pSec max	F = 156.25 MHz, Integration Bandwidth = 12 kHz to 20 MHz all Vdds

Notes:

- All min and max limits are specified over temperature and rated operating voltage with 15pF output unless otherwise stated.
- Typical values are at +25°C and nominal supply voltage.

Ordering Information:

Part Number Guide						
Packages	Input Voltage	Operating Temperature	Stability (ppm)	Output	Select Function	Frequency
IM842B – 5.0 x 3.2 IM842C – 3.2 x 2.5	1 = +1.8 V* 6 = +2.5 V 3 = +3.3 V (see Notes)	1 = 0°C to +70°C 2 = -40°C to +85°C 3 = -20°C to +70°C	E = ±10 F = ±20 A = ±25 Z = ±30 B = ±50	8 = LVDS 9 = LVPECL	H = Tri-state S = Standby	- Frequency

Notes:

- +1.8 V Supply Voltage (option 1) is for LVDS outputs only

Sample Part Number: IM842C-62F9S-100.0000MHz

This 100.0000 MHz oscillator in a 3.2 x 2.5 package with stability ±20 ppm from -40°C to +85°C using a supply voltage of +2.5 V. With an output waveform of LCPECL and Pin 1 functioning as Standby

Sample Part Number: IM842B-13Z8H-150.0000MHz

This 150.0000 MHz oscillator in a 5.0 x 3.2 package with stability ±30 ppm from -20°C to +70°C using a supply voltage of +1.8 V. . With an output waveform of LVDS and Pin 1 functioning as Tri-state.

Notes:

- Not all options are available at all frequencies and temperatures ranges.
- Please consult with sales department for any other parameters or options.
- Oscillator specification subject to change without notice.

List of Supported Frequencies (in MHz)							
25.000000	50.000000	74.175824	74.250000	75.000000	98.304000	100.000000	106.250000
125.000000	133.000000	133.300000	133.330000	133.333000	133.333300	133.333330	133.333333
148.351648	148.500000	150.000000	155.520000	156.250000	161.132800	166.000000	166.600000
166.660000	166.666000	166.666600	166.666660	166.666666	200.000000	212.500000	

Absolute Maximum Limits	
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage (Vdd)	-0.5 VDC to 4.0 VDC
Electrostatic Discharge	2000 V max
Solder Temperature (follow standard Pb free soldering guidelines)	260°C max
Junction Temperature	150°C max

Waveform Diagrams:

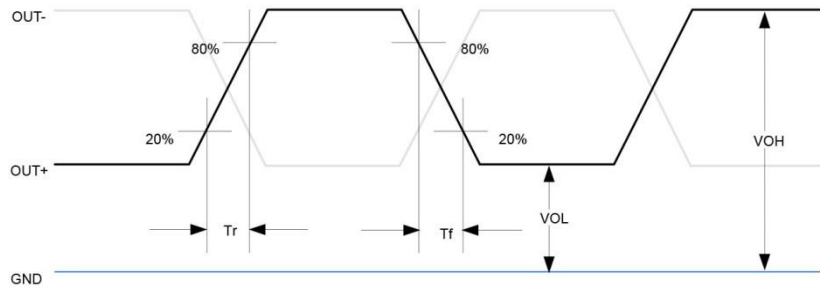


Figure 1(a): LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

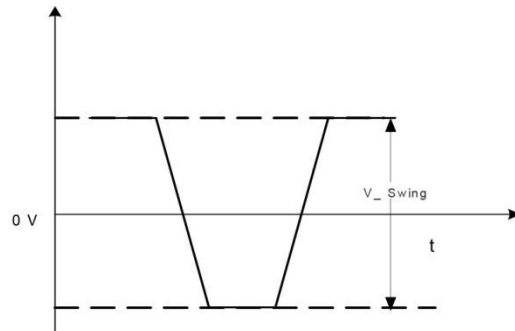


Figure 1(b): LVPECL Voltage Levels Across Differential Pair

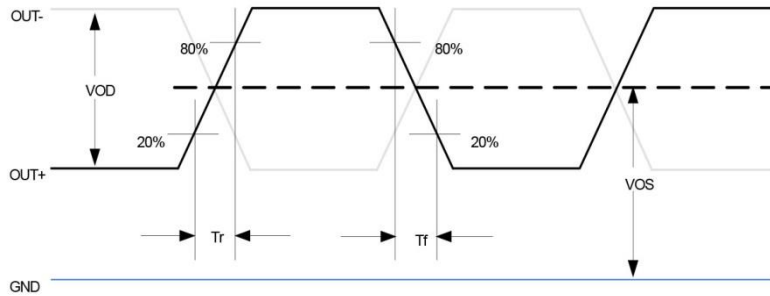


Figure 2: LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams – LVPECL:

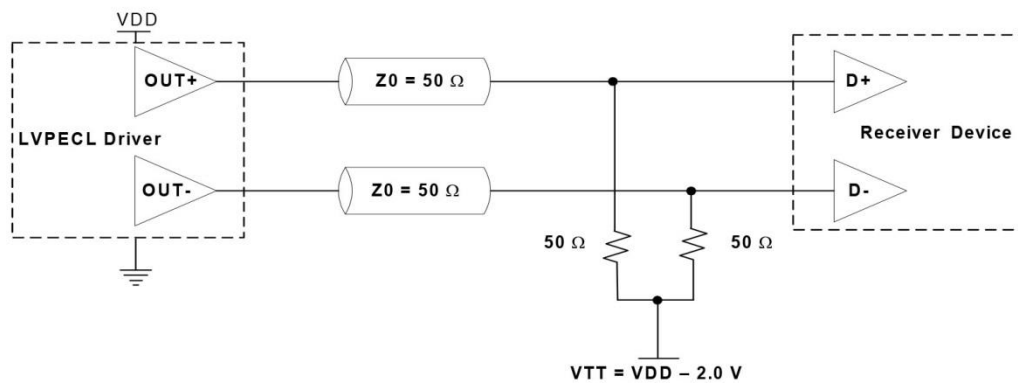


Figure 3: LVPECL Typical Termination

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IM842 Series

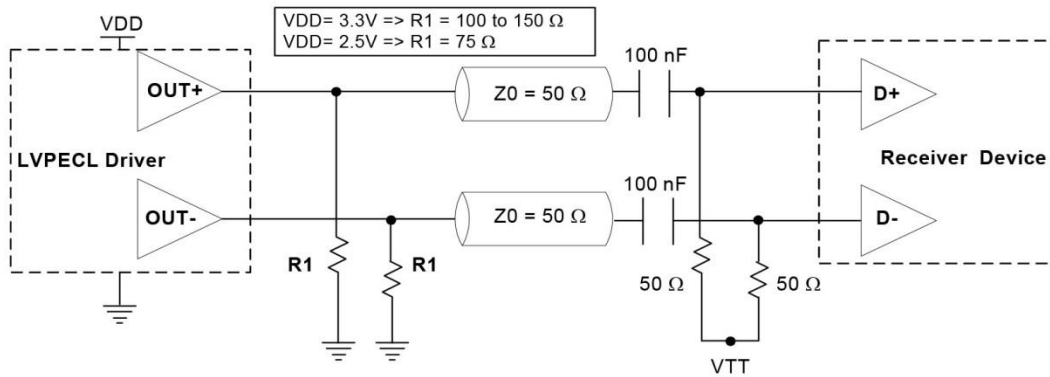


Figure 4: LVPECL AC Coupled Termination

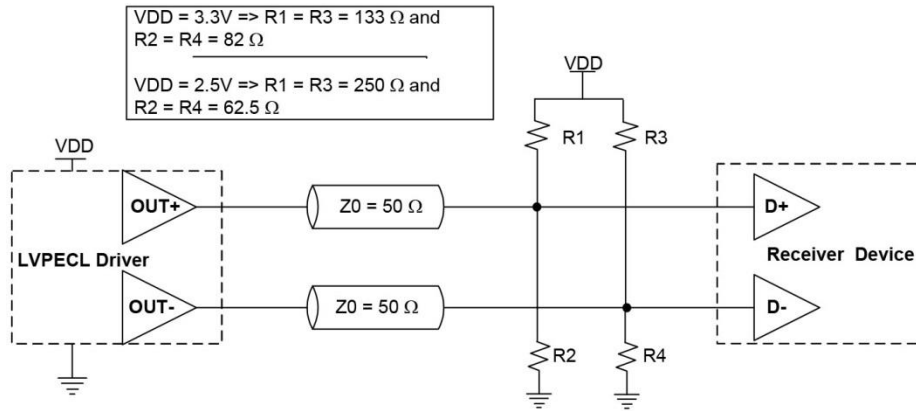


Figure 5: LVPECL with Thevenin Typical Termination

Termination Diagram – LVDS:

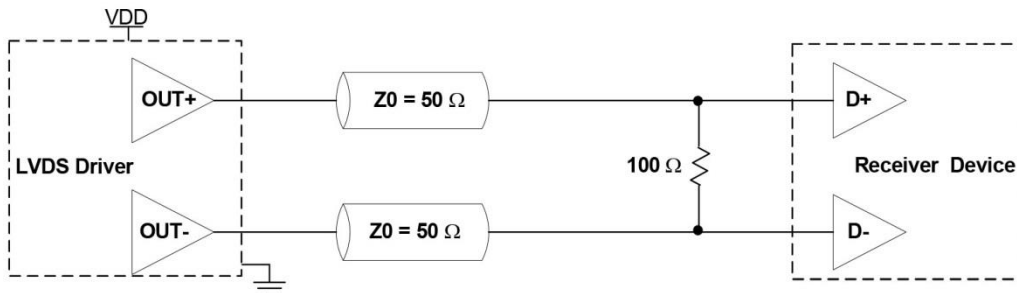
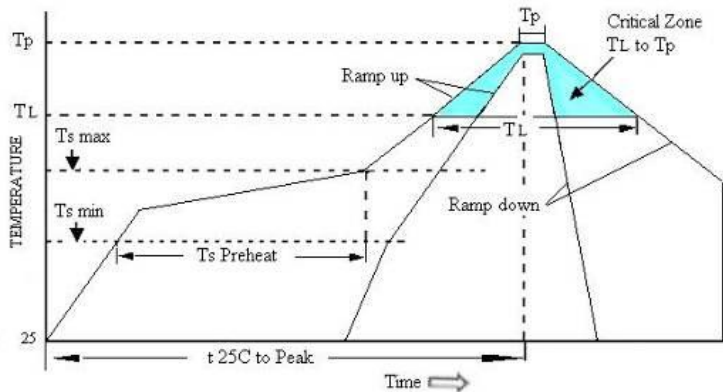


Figure 6: LVDS Single Termination (Load Terminated)

Environmental Specifications:

Environmental Compliance	
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL Level 1 at +260°C

Pb Free Solder Reflow Profile

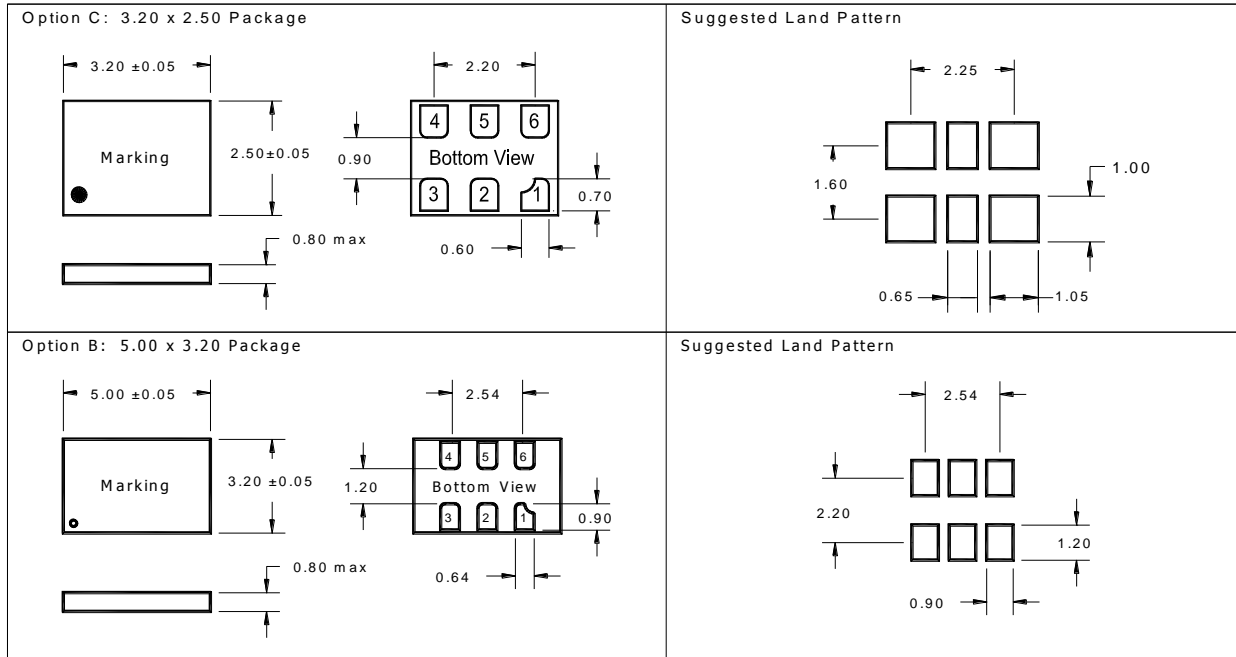


T _s max to T _L (Ramp-up Rate)	3°C / second max
Preheat	
Temperature min (T _s min)	150°C
Temperature typ (T _s typ)	175°C
Temperature max (T _s max)	200°C
Time (T _s)	60 to 180 seconds
Ramp-up Rate (T _L to T _p)	3°C / second max
Time Maintained Above Temperature (T _L)	217°C
Time (T _L)	60 to 150 seconds
Peak Temperature (T _p)	260°C max for seconds
Time within 5°C to Peak Temperature (T _p)	20 to 40 seconds
Ramp-down Rate	6°C / second max
Time 25°C to Peak Temperature	8 minute max
Moisture Sensitivity Level (MSL)	Level 1

Units are backward compatible with +240°C reflow processes

Mechanical Details:

Package Dimensions and Suggested Land Pattern



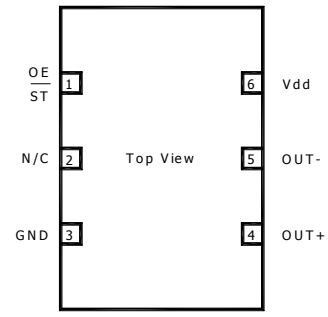
Marking

Line 1 = XXXXX (Lot code)
Dot to denote Pin 1 location

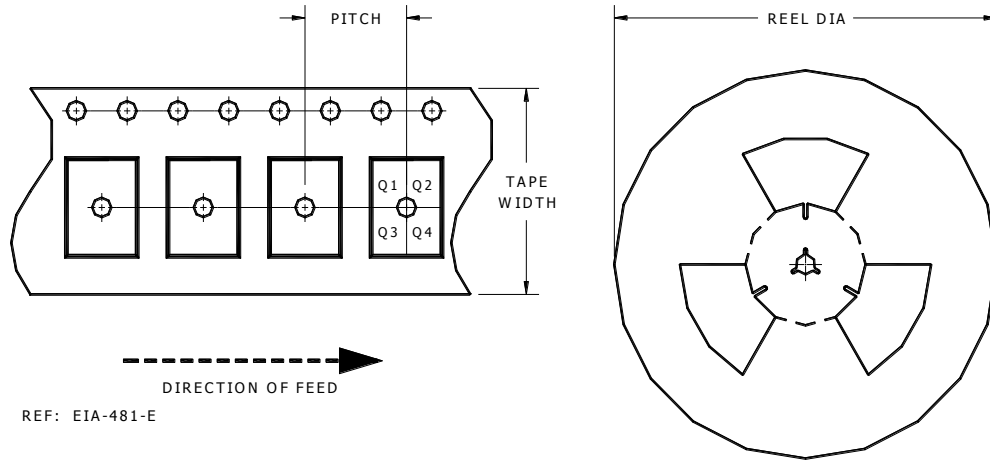
Package Information

Leadframe: C194
Plating: NiPdAu

Pin Functionally:

Pin	Symbol	Functionality		Pin Assignments
1	OE	Tri-state	High or Open = specified frequency output Low = Output is high impedance, only output is disabled.	
	\overline{ST}	Standby	High or Open = specified frequency output. Low = Output is low (weak pull down). Device goes to sleep	
2	NC	NA	No Connection: Leave it floating or connected to GND for better head dissipation	
3	GND	Power	Vdd – Power Supply Ground	
4	Out+	Output	Oscillator output	
5	Out-	Output	Complementary Oscillator output	
6	Vcc	Power	Power supply voltage	
Notes:				
1. In OE or \overline{ST} mode, a pull-up resistor of 10.0 kΩ or less is recommended if Pin 1 is not externally driven. If Pin 1 needs to be left floating, use the NC option.				
2. A capacitor of value 0.1 μF or higher between Pin 4 (Vcc) and Pin 1 (GND) is required.				

Tape and Reel Dimensions



Part Number	Size	Pitch	Tape Width	Pin Orient.	Reel Dia.	Count
IM842B	5.0 x 3.2	4.0 ± 0.1	8.3 max	Q1	180 Dia	3000
IM842C	3.2 x 2.5	4.0 ± 0.1	8.3 max	Q1	180 Dia	3000

Notes:

- All dimensions are in mm.
- Do not scale drawings.

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