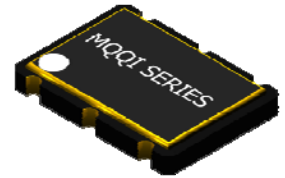


MQQI Series 5X7 Ceramic SMD Oscillator



- User Selectable Up to Four Frequencies
- LVDS, LVPECL OR CMOS
- 6 Pad Standard Package
- OneClock™



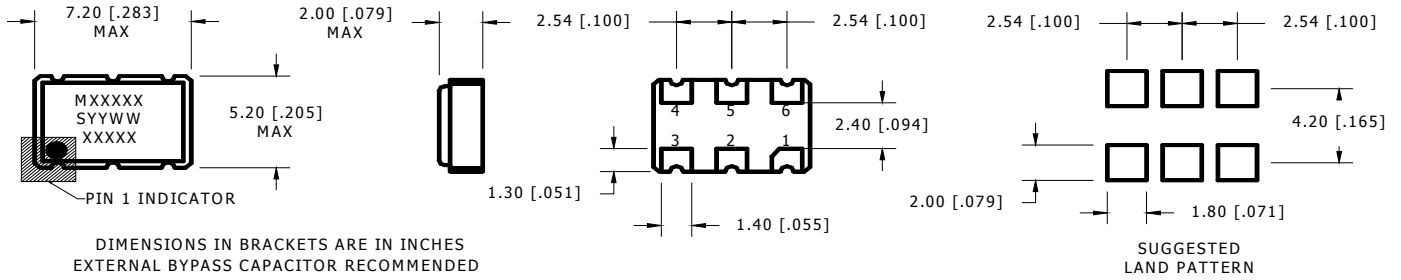
Frequency Range CMOS	10MHZ to 250MHZ					
Frequency Range LVDS & LVPECL	50.000MHZ to 1.50GHZ					
Temperature Stability*	(See Part Number Guide for Options)					
Operating Temperature Range	(See Part Number Guide for Options)					
Storage Temperature Range	-55°C to +125°C					
Aging (+25°C ±3°C)	±5ppm for first year					
Waveform	LVPECL		CMOS		LVDS	
Supply Voltage ±5% (Vdd)	+2.50 VDC	+3.30 VDC	+2.50 VDC	+3.30 VDC	+2.50 VDC	+3.30 VDC
Supply Current	54mA typ		20mA typ	25mA typ	23mA typ	
Load	50Ω		15pF	10 TTL Gates or 30pF	100Ω	
V _{ol}	.800V typ	1.60V typ	10% Vdd max		1.47V typ	1.60V typ
V _{oh}	1.50V typ	2.35V typ	90% Vdd min		2.15V typ	2.30V typ
Differential Voltage	.700V typ				.650V typ	.700V typ
Rise/Fall Time (10% to 90% of Supply Voltage)	250pSec max		4nSec		350pSec max	
Symmetry (50% of waveform)	(See Part Number Guide for Options)					
Start-up Time	10mSec max					
Period Jitter (RMS)	<2.5pSec					
Phase Jitter (12KHZ to 20MHZ)	<1.0pSec					
Tri-State Operation	V _{ih} = 70% of Vdd min to Enable Output V _{il} = 30% max or grounded to Disable Output (High Impedance)					
Tristate Current Consumption (Disabled)	16mA					
Absolute Maximum Voltage (Vdd)	4.20 Volts DC					
* Inclusive of Temperature., Load and Voltage						



MMD Monitor/Quartztek
 30400 Esperanza, Rancho Santa Margarita, CA, 92688
 Phone: (949) 709-5075, Fax: (949) 709-3536, www.mmdcomp.com
 Sales@mmdcomp.com



Mechanical Details



Pin Connections		Single Frequency
Pin 1	See Truth Table	Tristate
Pin 2**	See Truth Table	No Connection
Pin 3	Ground	Ground
Pin 4	Output	Output
Pin 5***	Complimentary Output ONLY LVPECL & LVDS	Complimentary Output ONLY LVPECL & LVDS
Pin 6	Supply Voltage	Supply Voltage

Dual Frequency Truth Table	
Pin 2	Corresponding Frequency
0	Frequency 1
1	Frequency 2

Quad Frequency Truth Table *		
Pin 1	Pin 2	Corresponding Frequency
'0'	'0'	Frequency 1
'0'	'1'	Frequency 2
'1'	'0'	Frequency 3
'1'	'1'	Frequency 4

'0' = GND
'1' = Vdd
*No tristate with 4 Frequency Option
**Tristate Option Available
*** CMOS is No Connection

Typical Phase Noise

Offset Frequency	CMOS 70.000MHZ	LVPECL/LVDS 160.000MHZ	LVPECL/LVDS 622.000MHZ
100Hz	-88dBc/Hz	-85dBc/Hz	-80dBc/Hz
1KHz	-115dBc/Hz	-100dBc/Hz	-97dBc/Hz
10KHz	-120dBc/Hz	-115dBc/Hz	-117dBc/Hz
100KHz	-125dBc/Hz	-118dBc/Hz	-128dBc/Hz
1MHz	-130dBc/Hz	-128dBc/Hz	-138dBc/Hz
10MHz	-145dBc/Hz	-145dBc/Hz	-145dBc/Hz

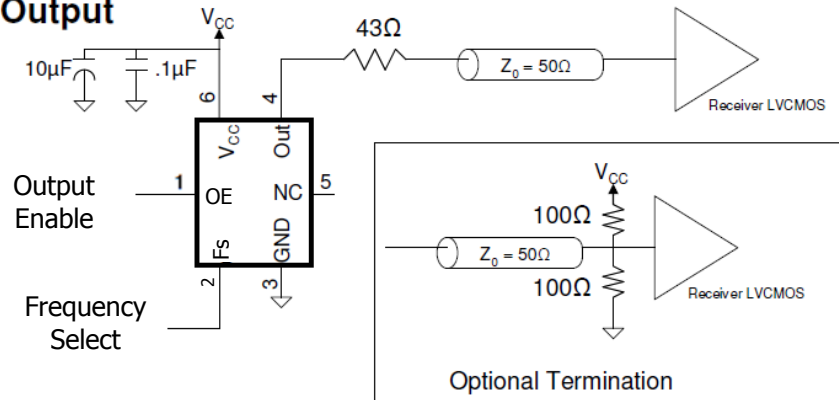


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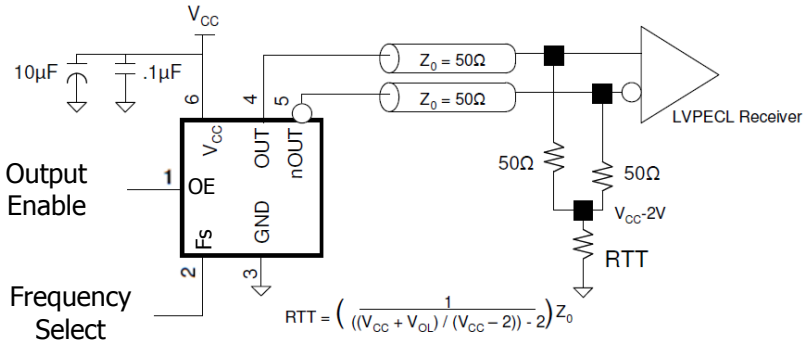


Test Set Up

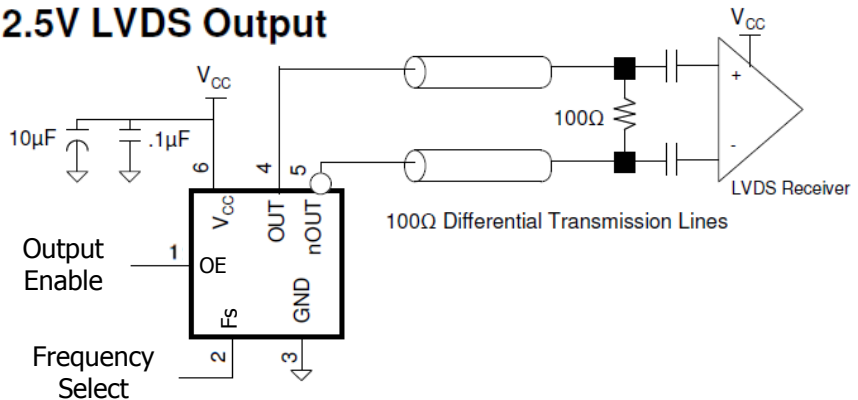
Termination for LVCMOS Output



Termination for 3.3V LVPECL Output



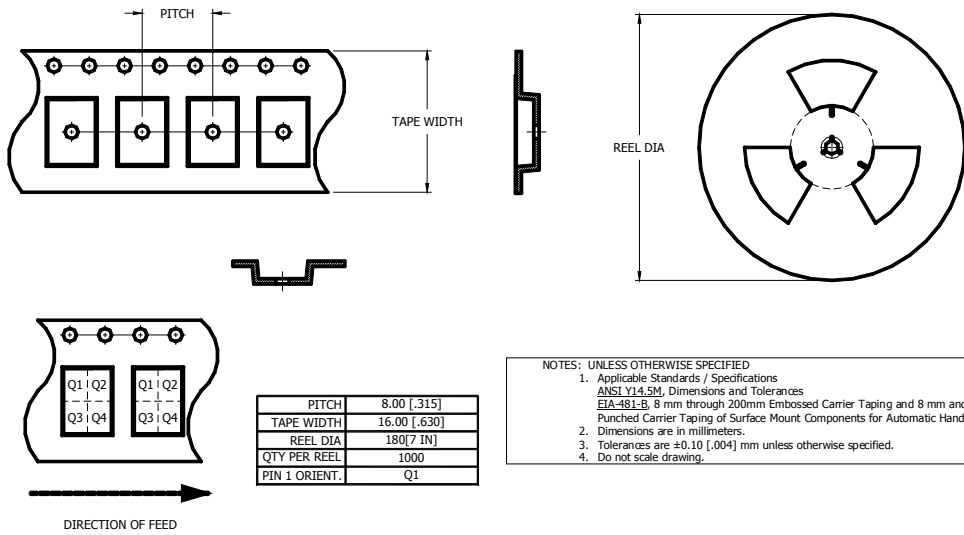
Termination for 3.3V and 2.5V LVDS Output



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Tape & Reel Dimensions



PITCH	8.00 [.315]
TAPE WIDTH	16.00 [.630]
REEL DIA	180[7.14]
QTY PER REEL	1000
PIN 1 ORIENT.	Q1

- NOTES: UNLESS OTHERWISE SPECIFIED
1. Applicable Standards / Specifications
ANSI Y14.5M, Dimensions and Tolerances
EIA-481-B, 8 mm through 200mm Embossed Carrier Taping and 8 mm and 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling.
 2. Dimensions are in millimeters.
 3. Tolerances are ± 0.10 [.004] mm unless otherwise specified.
 4. Do not scale drawing.



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